## Remarks

The preceding Amendment and following Remarks are submitted in response to the non-final Office Action mailed January 16, 2002, setting a three-month shortened statutory period for response ending April 16, 2002. Claims 1-23 are pending in the Application, with claims 20-23 being newly presented. Reconsideration, examination and allowance of all pending claims are respectfully requested.

Claims 1-2, 4-6 and 14-18 were rejected under 35 U.S.C. § 102(e) as being anticipated by *Atobe et al.* (U.S. Patent No. 6,271,955). With respect to claim 1, the Examiner states that *Atobe et al.* suggest a method for making a thin silicon structure comprising the steps of providing a glass substrate and a silicon substrate having two planar surfaces; forming a recess in the glass substrate; bonding the silicon substrate to the glass substrate such that at least part of the silicon wafer bonds the glass wafer, and part of the silicon wafer overhangs the recess; and selectively removing a portion of the silicon substrate to form an overhanging structure. The Examiner further states that "layer 112 is just a doped portion of the silicon layer and thus is still the silicon substrate surface."

After careful review Applicants respectfully submit that the *Atobe et al.* reference does not anticipate or render obvious the method recited in claim 1 or claim 14. *Atobe et al.* clearly suggest separately forming the silicon mirror substrate and the glass substrate before bonding the two together (see, for example, *Atobe et al.*, column 16, line 41 to column 18, line 16).

In contrast, claim 1 of the present invention recites:

> 1. (Amended) A method for making a thin silicon structure comprising the steps of:
>
> providing a glass wafer or substrate;
>
> providing a silicon wafer having a first substantially planar surface and a second substantially planar surface;
>
> forming a recess in said glass wafer or silicon wafer first surface;
>
> bonding said silicon wafer to said glass wafer such that at least part of said silicon wafer first surface bonds to said glass wafer and at least part of said silicon wafer first surface overhangs said recess; and
>
> after said bonding step, selectively removing a portion of said silicon wafer from said silicon wafer second surface through to said silicon wafer first surface such that a silicon structure is formed overhanging said recess.

As can be seen, and unlike *Atobe et al.*, the bonding step of claim 1 is performed before the selectively removing step. To make this more clear, however, Applicants have amended claim 1

to recite that the selectively removing step is performed after said bonding step. Claim 14 has been similarly amended. In view of the foregoing, Applicants believe that claims 1 and 14, and dependent claims 2-6 and 14-19, are clearly patentable over *Atobe et al.*

Applicants have added newly presented claims 20-23. Newly presented claim 20 recites "after said securing step, selectively removing a portion...". Thus, for similar reasons given above with respect to claim 1 and other reasons, claim 20 is believed to be clearly patentable over *Atobe et al.*

Newly presented claim 21 recites:

> 21. (Newly Presented) A method for making a thin structure comprising the steps of:
>
> providing a first substrate having a first substantially planar surface and a second substantially planar surface;
>
> providing a second substrate having a first substantially planar surface and a second substantially planar surface;
>
> forming a recess in said first substantially planar surface of said first substrate and/or said first substantially planar surface of said second substrate;
>
> securing said first substrate to said second substrate such that said first substantially planar surface of said first substrate faces said first substantially planar surface of said second substrate; and
>
> selectively removing a portion of said first substrate from said second substantially planar surface of said first substrate such that a thin structure is formed overhanging said recess, said thin structure being doped at a concentration of between zero and $1x10^{18}$ atm/cm$^3$.

As can be seen, newly presented claim 21 recites that the thin structure that overhangs the recess is doped at a concentration of between zero and $1x10^{18}$ atm/cm$^3$. Note that newly presented claim 21 is not limited to performing the selectively removing step after the securing step. In any event, and in contrast to claim 21, *Atobe et al.* appear to suggest providing a heavily doped thin silicon structure (at least $1x10^{18}$ atm/cm$^3$) so that the boron doped layer 112 can be made to function as an etching stop layer. *Atobe et al.* state:

> As a result, the boron (B) of the boron dopant was thermally diffused into the silicon substrate 110, and on the lower surface of the silicon substrate 110 the boron doped layer 112 shown in FIG. 4B was formed. The thickness of the boron doped layer 112 can be adjusted in this thermal diffusion step by varying the time and temperature conditions, and in this embodiment, by carrying out thermal diffusion for 6 hours at 1000°C. a boron doped layer 112 of thickness 2 to 3 mm was formed.

In this case, the boron concentration in the boron doped layer 112 is preferably at least $1x10^{18}$ atm/cm$^3$. In this way, in the step of etching the silicon substrate 110 described below, the boron doped layer 112 can be made to function as an etching stop layer.

(Emphasis added) (*Atobe et al.*, column 12, lines 52-65). However, and as noted in the present specification, this approach has a number of disadvantages:

> The aforementioned structures are often made starting with a silicon wafer substrate. A boron-doped silicon epitaxial layer is then grown on the silicon wafer substrate and is subsequently patterned in the desired shape. As is further described below, the boron is used as an etch stop in later processing to allow for easy removal of the silicon substrate, leaving only the thin boron-doped epitaxial layer.
>
> At the interface between the boron-doped epitaxial layer and the silicon substrate, the boron tends to diffuse out of the epitaxial layer and into the silicon substrate. This depletes the epitaxial layer of some boron, and enriches the silicon substrate with boron. The epitaxial layer thus often has a reduced concentration of boron near the interface, which is sometimes called the "boron tail."
>
> After the boron-doped silicon epitaxial layer has been grown to the desired thickness, the silicon substrate is often removed using an etchant that is boron selective. Specifically, the etchant will etch away the silicon substrate, but not the boron-doped silicon epitaxial layer. One such etchant is a solution of ethylene diamine, pyrocatechol, and water (EDP). The etchant typically etches the silicon at a fast rate up to a certain high level boron concentration, at which point the etch rate significantly slows. This high boron concentration level is termed the etch stop level.
>
> The boron concentration near the epitaxial layer surface having the boron tail may be lower than the etch stop level, allowing the etching to remove some of the epitaxial layer surface at a reasonable rate, stopping at the etch stop level of boron concentration beneath the initial surface. The resulting boron-doped structure, such as a beam, thus has two surfaces, the silicon side surface that has the boron tail and the airside surface that has a boron surface layer concentration substantially equal to the concentration in the bulk of the beam away from either surface. Thus, the opposing surfaces have different boron surface layer concentrations.
>
> The building of a suspended element often includes using an epitaxially grown single-crystal silicon heavily doped with boron, for example, greater than ten to the twentieth atoms per cubic centimeter ($10^{20}$/cm$^3$). In some applications, this doped material may present problems. One problem is an intrinsic tensile stress, which, when the boron-doped layer is relatively thick, can produce severe wafer bow. This wafer bow is incompatible with some fabrication steps. Another problem is that the thickness of the epitaxial layer may be limited due to technological reasons, for example, deposition conditions. Yet another problem is that the Young modulus of the boron-doped material may be lower than that of

silicon, and may not be well known and understood.

In addition, the intrinsic losses of the boron-doped material may be higher than those of low-doped silicon. In the lost wafer process, the final release of the mechanical structure is often performed using a long, wet-etching step, which can be based on ethylene-diamine-pyrocathacol (EDP) solution, which requires careful control to maintain industrial hygiene standards during manufacture. What would be desirable is a fabrication process that eliminates the need for highly doped silicon and does not require a wet-etching step using EDP.

(Emphasis added). By providing a thin structure that overhangs the recess, wherein the thin structure has a doping concentration of between zero and $1x10^{18}$ atm/cm$^3$ as recited in claim 21, many of the disadvantages of *Atobe et al.* may be obviated. In view of the foregoing, Applicants believe that claim 21 is clearly patentable over *Atobe et al.*

Newly presented claim 22 is an apparatus claim that recites "the one or more openings defining a thin structure that overhangs said cavity, said thin structure being doped at a concentration of between zero and $1x10^{18}$ atm/cm$^3$". Thus, for similar reasons given above with respect to claim 21, Applicants believe that newly presented claim 22 is also clearly patentable over *Atobe et al.*

Newly presented claim 23 is similar to claim 19, but with several limitations removed. The Examiner objected to claim 19 as being dependent upon a rejected base claim, but indicated that claim 19 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Since claim 19 is believed to clearly allowable over the cited art, newly presented claim 23 is also believed to be in condition for allowance.

**Allowable Subject Matter**

On page 3 of the Office Action, the Examiner states that claims 7-13 are allowed. The Examiner further states that claim 19 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form to include all of the limitations of the base claim and any intervening claims. Because independent claim 14 is believed to be in condition for allowance, claim 19 is also believed to be in condition for allowance.

Attached hereto is a marked-up version of the changes made to the claims by the current Amendment. The attached page is captioned "**Version With Markings To Show Changes Made.**"

In view of the foregoing, all pending claims 1-23 are believed to be in condition for allowance. Reexamination and reconsideration are respectfully requested. If the Examiner would like to discuss the application or its examination in any way, please call the undersigned attorney at (612) 677-9050.

Respectfully submitted,

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By Their Attorney,

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**Version With Markings To Show Changes Made**

In the Claims:

Claims 1, 14 and 19 have been amended as follows:

1. (Amended) A method for making a thin silicon structure comprising the steps of:

providing a glass wafer or substrate;

providing a silicon wafer having a first substantially planar surface and a second substantially planar surface;

forming a recess in said glass wafer or silicon wafer first surface;

bonding said silicon wafer to said glass wafer such that at least part of said silicon wafer first surface bonds to said glass wafer and at least part of said silicon wafer first surface overhangs said recess; and

after said bonding step, selectively removing a portion of said silicon wafer from said silicon wafer second surface through to said silicon wafer first surface such that a silicon structure is formed overhanging said recess.

14. (Amended) A method for making a thin structure, comprising:

providing a first wafer or substrate;

providing a second wafer having a first substantially planar surface and a second substantially planar surface;

forming a recess in said first wafer substrate;

bonding said second wafer to said first wafer such that at least part of said second wafer first surface bonds to said first wafer so that at least part of said second wafer first surface overhangs said recess; and

after said bonding step, selectively removing a portion of said second wafer from said second wafer second surface through to said second wafer first surface such that a thin structure is formed overhanging said recess.

19. (Amended) A method for making a thin structure as in claim 14, further comprising:

providing a patterned metal layer on the first substantially planar surface of the second wafer, such that the metal layer is patterned to coincide with said recess;

stopping the selective [etching] removal step at or near said metal layer to form the thin structure; and

removing said metal layer.